

FIG. 1

FIG. 1

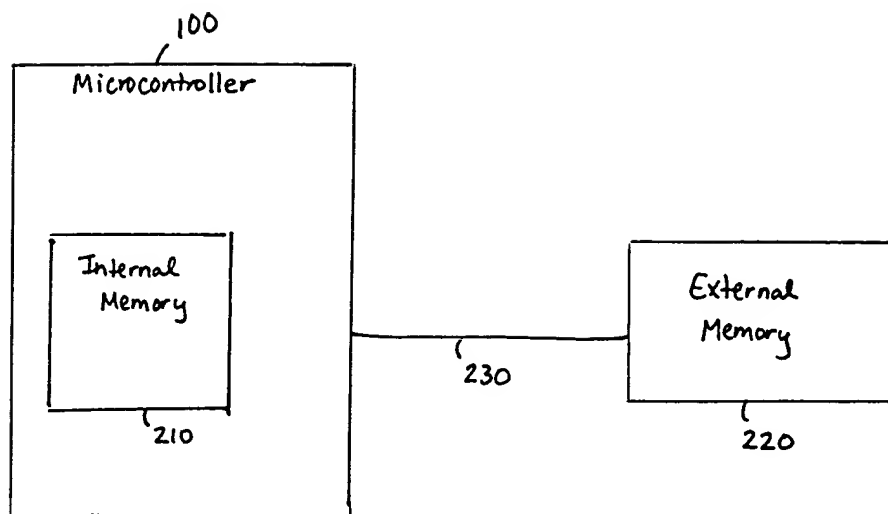


FIG. 2

FIG. 3

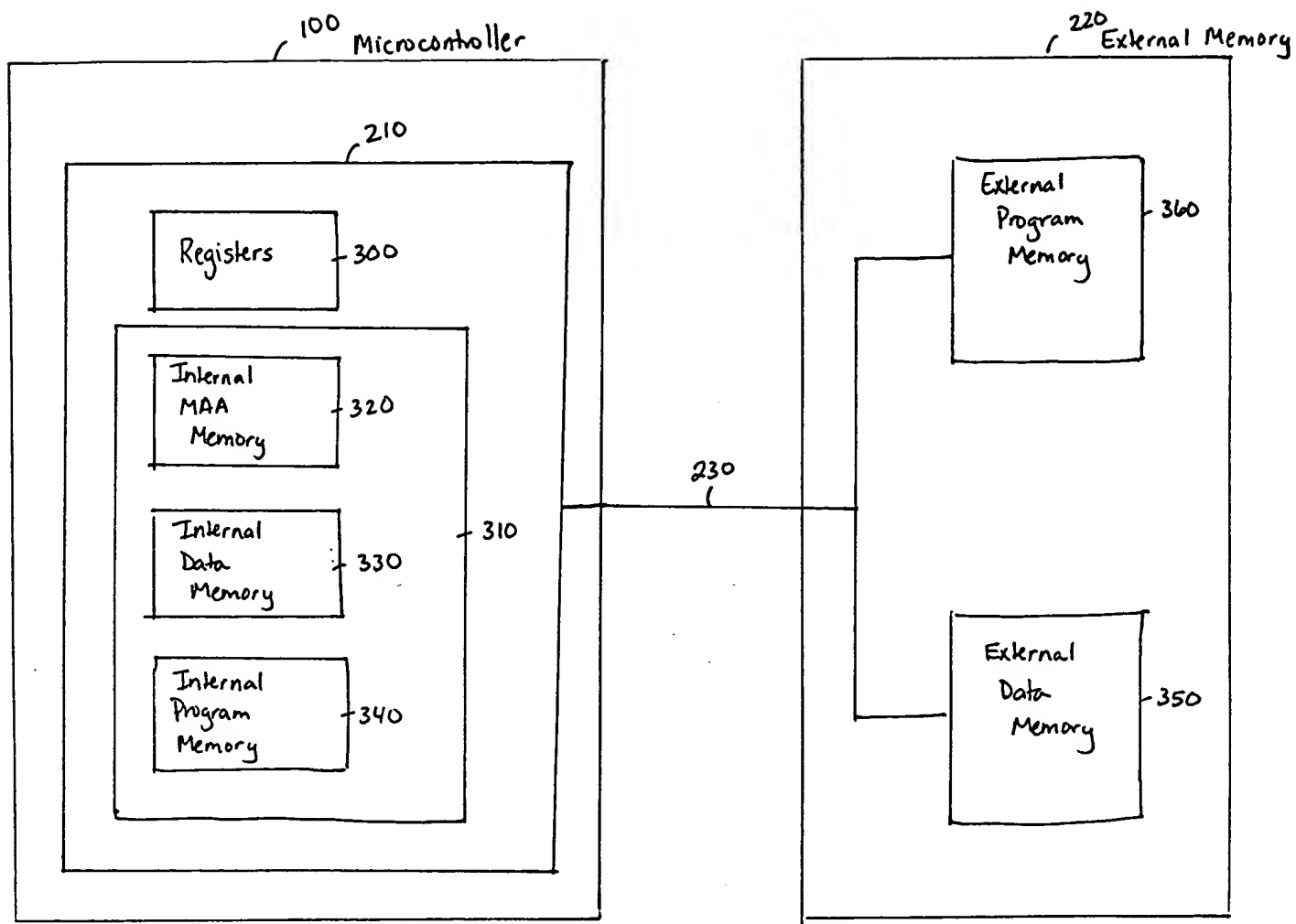


FIG. 3

210

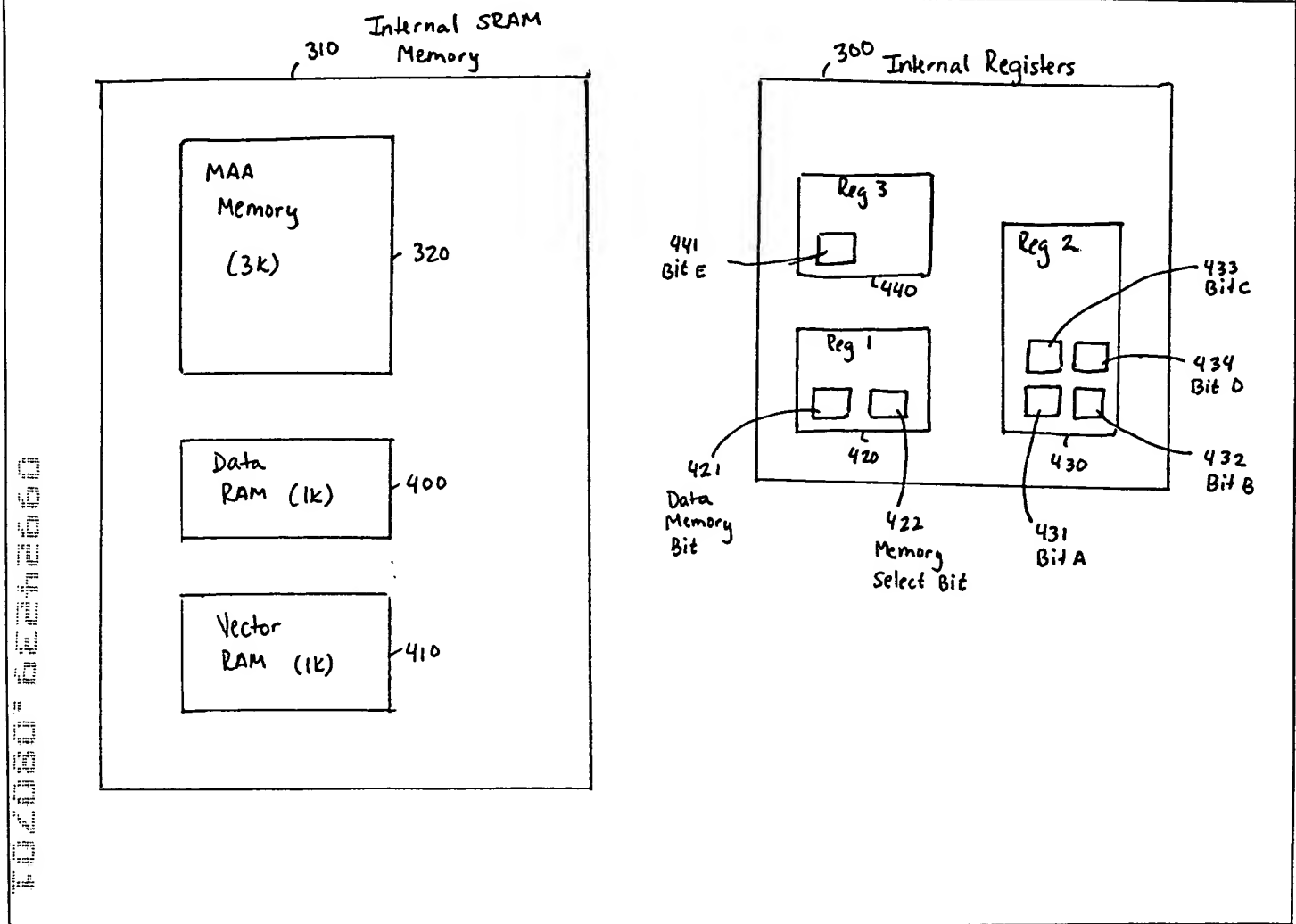


FIG. 4

```
graph TD; 500[Setting a Bit in a Register] --> 510[Providing a 1st Memory]; 510 --> 520[Providing a 2nd Memory]; 520 --> 530[Alter Contents of 2nd Memory]; 530 --> 540[Change the bit in Register]; 540 --> 550[Interchange logical location of 1st Memory w/ 2nd Memory];
```

FIG. 5

FIG. 6

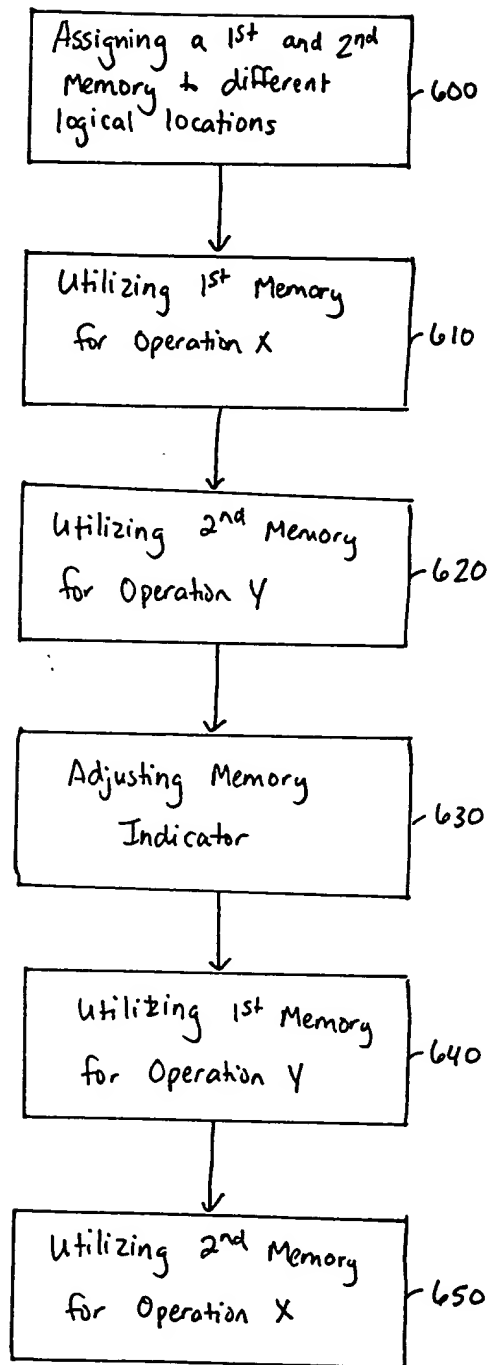


FIG. 6

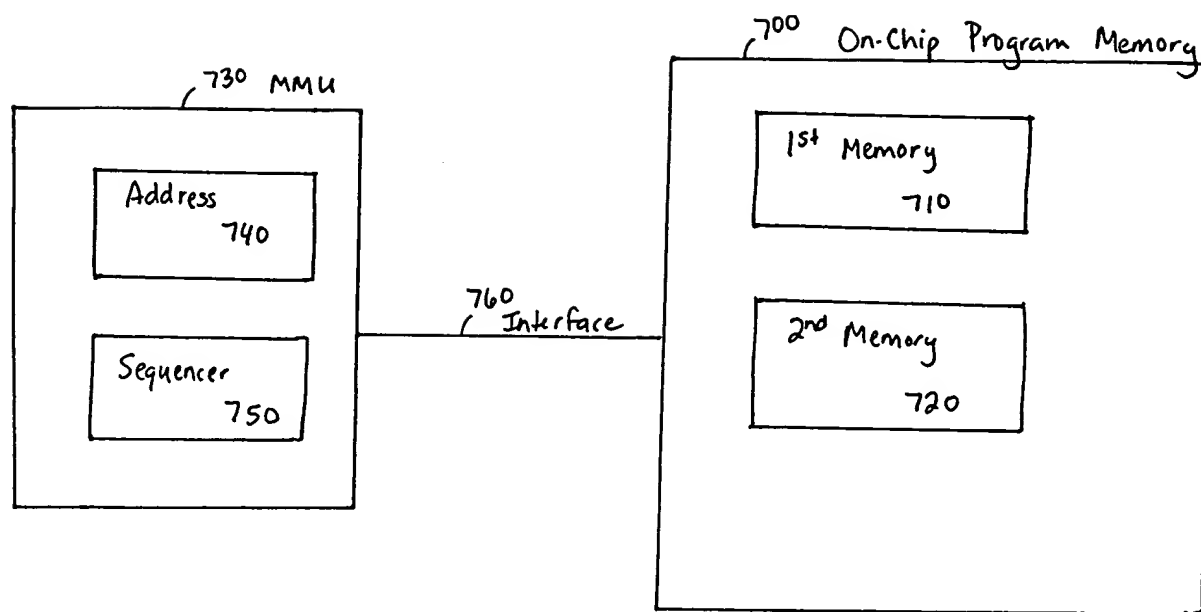


FIG. 7